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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/976,635	10/12/2001	Jigish G. Trivedi	MI22-1771	1649

21567 7590 06/04/2003

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EXAMINER
PHAM, THANHHA S

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/04/2003

10

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,635	TRIVEDI, JIGISH G.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-12 and 36-39* is/are allowed.

6)☒ Claim(s) *13-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action responses to Applicant's Amendment in Paper No. 10 dated 3/7/03.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Ochii [US 4,661,202].

Ochii, fig 3's and 6 and related text col 1-8, discloses the claimed method of forming a local interconnect comprising:

forming an isolation trench (24, fig 3A, , col 4 lines 30-40) within semiconductive material of a semiconductor substrate (21), the semiconductive material having an outer surface;

depositing a trench isolation material (26, fig 3A, col 4 lines 30-40) over the semiconductor substrate and to within the isolation trench;

removing trench isolation material effective to form a line trench (fig 3B, col 4 lines 40-44) within the trench isolation material into a desired local interconnect configuration, the line trench having a base which is lower than the outer surface, said

removing forming at least a portion of the line trench to be laterally centered between sidewalls of the isolation trench in at least one cross section;

forming a first conductive material (46, fig 6 related to fig 3C, col 4 lines 45-52 and col 5 lines 51-63) to within the line trench to form a conductive lining within the line trench; and

depositing a second conductive material (doped polycrystalline siicon 49, fig 6, col 4 lines 45-52 and col 5 lines 51-63) different from the first conductive material on the conductive lining and to within the trench line.

2. Claims 17-18 and 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Yusuke Kohyama [EP-0457131].

Yusuke Kohyama, fig 4's and text col 1-7, discloses the claimed method of forming a local interconnect comprising:

forming an isolation trench (groove formed by etching the substrate 1, fig 4A, col 3 lines 21-24) within semiconductive material of a semiconductor substrate (1), the semiconductive material having an outer surface;

depositing a trench isolation material (4, fig 4A, col 3 lines 24-33) over the semiconductor substrate and to within the isolation trench;

removing trench isolation material from within the isolation trench effective to form a line trench (fig 4B, col 3 lines 34-38) within the trench isolation material into a desired local interconnect configuration, the line trench having a base which is lower than the outer surface, said removing forming at least a portion of the line trench to be laterally centered between sidewalls of the isolation trench in at least one cross section;

forming an oxidation resistant liner material (5, fig 4B, col 3 lines 3 lines 29-45) to within the line trench to form an oxidation resistant lining within the line trench, the oxidation resistant lining material being insulative;

depositing a conductive material (7, fig 4C, col 3 lines 46-63) to within the line trench and on the oxidation resistant lining; and

covering the conductive material with insulative material (8, fig 4D, col 4 lines 13-24) the same as the trench isolation material wherein at least some of the insulative material is received within the line trench and on the conductive material.

3. Claims 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Yusuke Kohyama [EP-0457131].

Yusuke Kohyama, fig 4's and text col 1-7, discloses the claimed method of forming a local interconnect comprising:

forming an isolation trench (groove formed by etching the substrate 1, fig 4A, col 3 lines 21-24) within semiconductive material of a semiconductor substrate (1), the semiconductive material having an outer surface, the isolation trench having opposing longitudinal sidewalls in at least one cross section;

depositing a trench isolation material (4, fig 4A, col 3 lines 24-33) over the semiconductor substrate and to within the isolation trench;

removing trench isolation material from within the isolation trench effective to form a line trench (fig 4B, col 3 lines 34-38) within the trench isolation material into a desired local interconnect configuration which is laterally centered between the

opposing isolation trench sidewalls in the one cross section, the line trench having a base which is lower than the outer surface;

forming a conductive material (7, fig 4C, col 3 lines 46-63) to within the line trench; and

after forming the conductive material, forming insulative material (8, fig 4D, col 4 lines 13-24) within the line trench below the outer surface.

With respect to claim 24, Yusuke Kohyama (figs 4C-4D) discloses forming the conductive material within the line trench comprising depositing conductive material and recessing it within the line trench after the depositing (the conductive material being recessed by formation of the insulative material 8).

4. Claims 32 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Yusuke Kohyama [EP 0457131].

Yusuke Kohyama, fig 4's and text col 1-7, discloses the claimed method of forming a local interconnect comprising:

filling an isolation trench (3, fig 4A, col 3 lines 21-29) formed relative to an outer surface of a semiconductive material of a semiconductor substrate (1) with trench isolation material (4)

etching a line trench (fig 4B, col 3 lines 34-38) into a desired line configuration within trench isolation material (4) formed relative to an outer surface of semiconductive material of a semiconductor substrate (1), the line trench (trench defined by isolation material 4 below contact window 6, fig 4B) in the trench isolation material (4) not having a width which extends to active area substrate material in at least on cross section, the

line trench having an insulative base which is lower than the outer surface of the semiconductive material; and

forming conductive material (7, fig 4C, col 3 lines 46-63) over the semiconductor substrate which at least partially fills the trench.

With respect to claim 34, Yusuke Kohyama (figs 4C-4D) discloses forming the conductive material within the line trench comprising depositing conductive material and recessing it within the line trench after the depositing (the conductive material being recessed by formation of the insulative material 8).

5. Claims 32 and 35 are rejected under 35 U.S.C. 102(b) as being anticiapted by Ochii et al [US 4,661,202].

Ochii et al, figs 3's-6, discloses the claimed method of forming a local interconnect comprising:

filling an isolation trench (25, fig 3A) formed relative to an outer surface of a semiconductive material of a semiconductor substrate with trench isolation material (26);

etching a line trench (fig 3B, col 3 lines 24-38) into a desired line configuration within trench isolation material (26b) formed relative to an outer surface of semiconductive material of a semiconductor substrate, the line trench in the trench isolation material (26b) not having a width which extends to active area substrate material in at least on cross section, the line trench having an insulative base which is lower than the outer surface of the semiconductive material; and

forming conductive material (28, fig 3C) over the semiconductor substrate which at least partially fills the trench.

With respect to claim 35, Ochii (fig 3C and col 4 lines 53-57 and col 5 lines 51-63) discloses forming the conductive material (28) within the line trench comprising depositing at least two different composition conductive material (high melting point metal and impurity-doped polysilicon) to within the line trench.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yusuke Kohyama [EP 0457131] in view of Ochii [US 4,661,202].

Yusuke Kohyama, fig 4's and text col 1-7, substantially discloses the claimed method of forming a local interconnect comprising:

forming an isolation trench (groove formed by etching the substrate 1, fig 4A, col 3 lines 21-24) within semiconductive material of a bulk semiconductor substrate (1), the bulk semiconductor substrate having an outer surface,

depositing a trench isolation material (4, fig 4A, col 3 lines 24-33) over the bulk semiconductor substrate and to within the isolation trench;

removing trench isolation material from within the isolation trench effective to form a line trench (fig 4B, col 3 lines 34-38) within the trench isolation material into a desired local interconnect configuration which is laterally centered between the opposing isolation trench sidewalls in the one cross section, , the line trench having a base which is lower than the outer surface;

forming a conductive material (7, fig 4C, col 3 lines 46-63) to within the line trench; and

after forming the conductive material, forming insulative material (8, fig 4D, col 4 lines 13-24) within the line trench below the outer surface.

Yusuke Kohyama does not expressly teach: providing a bulk semiconductor substrate having a first conductivity type, an adjacent second conductivity type background region and a boundary extending between; and forming said isolation trench along the boundary.

However, forming the isolation trench along the boundary between the first and second conductivity type regions has been known in the art. See Ochii (fig 14 and col 6-8) as an evidence that shows formation of a isolation trench formed along a boundary extending between the first conductivity type background region (P-well) and the second conductivity type background region (N-well) where an local interconnection being formed in the isolation trench.

Therefore, it would have been obvious for those skilled in the art to modify the process of Yusuke Kohyama by providing the bulk semiconductor substrate and forming the isolation trench within the bulk semiconductor substrate and along the boundary

between the first and second conductivity type background regions, as being claimed, per taught by Ochii, to provide appropriate local interconnection as being needed in the isolation trench located between the first and second conductivity type regions.

With respect to claims 28-30, those skilled in the art would recognize that the combination process of Yusuke Kohyama and Ochii would provide a local interconnect structure wherein the isolation trench and the line trench being laterally centered over the boundary between the first and second conductivity type background regions.

With respect to claim 31, Yusuke Kohyama (fig 4B) teaches forming the line trench being laterally centered between longitudinal sidewalls of the isolation trench in at least one cross section.

7. Claims 13-16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yusuke Kohyama [EP 0457131] in view of Kang et al [US 6,287,965].

Yusuke Kohyama, fig 4's and text col 1-7, substantially discloses the claimed method of forming a local interconnect comprising:

forming an isolation trench (groove formed by etching the substrate 1, fig 4A, col 3 lines 21-24) within semiconductive material of a semiconductor substrate (1), the semiconductive material having an outer surface;

depositing a trench isolation material (4, fig 4A, col 3 lines 24-33) over the semiconductor substrate and to within the isolation trench;

removing trench isolation material from within the isolation trench effective to form a line trench (fig 4B, col 3 lines 34-38) within the trench isolation material into a

desired local interconnect configuration, the line trench having a base which is lower than the outer surface, said removing forming at least a portion of the line trench to be laterally centered between sidewalls of the isolation trench in at least one cross section;

forming an oxidation resistant liner material (5, fig 4B, col 3 lines 3 lines 29-45) to within the line trench to form an oxidation resistant lining within the line trench;

depositing a second conductive material (7, doped polysilicon, fig 4C, col 3 lines 46-63) to within the line trench and on the oxidation resistant lining; and

covering the second conductive material with insulative material (8, fig 4D, col 4 lines 13-24) the same as the trench isolation material wherein at least some of the insulative material is received within the line trench and on the conductive material.

Yusuke Kohayama does not teach forming the oxidation resistant liner material by using a first conductive material being different to the second conductive material (doped polysilicon). Instead, Yusuke Kohayama teaches the oxidation resistant liner material being of an insulative material.

However, Kang et al (fig 7C and col 8 lines 14-26) discloses the oxidation resistant liner material being of the first conductive material (214, AlTiN) having a improved thermal and oxidation resistant characteristics.

Therefore, it would have been obvious for those skilled in the art to modify process of Yusuke Kohayama by using the oxidation resistant liner material of the first conductive material (TiAlN) different to the second conductive material (doped polysilicon), as being claimed, per taught by Kang et al, to provide a better local interconnection structure with better conductance and improved oxidation resistance.

8. Claims 13, 25 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yusuke Kohyama [EP 0457131] in view of Liaw [US 5,920,098].

Yusuke Kohyama substantially discloses the claimed method of forming a local interconnection including forming a conductive material (7, fig 4C) to within the line trench. Yusuke Kohyama does not expressly teach forming said conductive material comprising depositing at least two different composition conductive materials to within the line trench.

However, using at least two different composition conductive materials for forming local interconnection has been known in the art. See Liaw as an evidence that shows forming local interconnect (14/15, fig 7, col 5 lines 6-35) by depositing at least two different composition conductive materials to within the line trench.

Therefore, it would have been obvious for those skilled in the art to modify process of Yusuke Kohyama by depositing at least two different composition conductive materials to within the line trench, as taught by Liaw, to form the local interconnect structure with two different composition conductive materials as a device being needed. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co., Inc. v. Interchemical Corp. , 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." (65 USPQ at 301).

9. Claims 26 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochii [4,661,202] or Yusuke Kohyama [EP 0457131] as applied to claims 23

and 32 above, in further view of Wolf et al ["Silicon Processing For the VLSI ERA", Vol 1 Process technology, pp 5-6, Lattic Press 1986].

Ochii, Kim and Yusuke Kohyama substantially discloses the claimed method but is silent about the teaching of using the semiconductor substrate of monocrystalline substrate.

However, Wolf et al shows that utilizing monocrystalline substrate keeps an important role in forming a semiconductor device due to its high crystalline perfection and uniformity of structure. In addition, using such as semiconductor substrate with moncrystalline structure has been well-known in the art of forming a semiconductor device.

Therefore, it would have been obvious for those skilled in the art to combine the teaching of Wolf et al to the process of Ochii, Kim or Yusuke Kohyama to use the semiconductor substrate of monocrystalline substrate for forming a better semiconductor device with reasons given above.

Allowable Subject Matter

10. Claims 1-12 and 36-39 allowed.

11. The following is a statement of reasons for the indication of allowable subject matter: Independent claims 1 and 5 recites the steps for forming local interconnect comprising: depositing a first trench isolation material over the semiconductor substrate and to within the isolation trench; removing first isolation material effective to form a line trench within the isolation first trench isolation material into a desired local interconnect

configuration; forming conductive material within the line trench; depositing a second trench isolation material over the first trench isolation material, over the conductive material within the isolation trench and within the line trench; and removing at least some first and second trench isolation material form the semiconductor substrate in at least one common removing step. However, such a combination of step is not suggested or taught by prior art. In addition, independent claim 36 recites the steps of forming local interconnect comprising: etching a line trench into a desired line configuration within trench isolation material formed relative to an outer surface of semiconductor material of a semiconductor substrate, the line trench in the trench isolation material not having a width which extends to active area substrate material in at least one cross section, the line trench having an insulative base which is lower than the outer surface; forming conductive material over the semiconductor substrate which at least partially fills the line trench; forming insulative material over the isolation material and over conductive material and to within the isolation trench; etching a contact opening into the insulative material which bridges over and between said active area substrate material and said conductive material; and forming a conductor within the contact opening which electrically connects said conductive material with said active area substrate material. However, such a combination of step is not suggested or taught by prior art.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (703) 308-6172. The examiner can normally be reached on Monday-Thursday 8:00 AM - 7:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-3432 for regular communications and (703) 308-7725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thanhha Pham
June 1, 2003

SUPERVISORY PRIMARY EXAMINER
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